Sierra Components, Inc.

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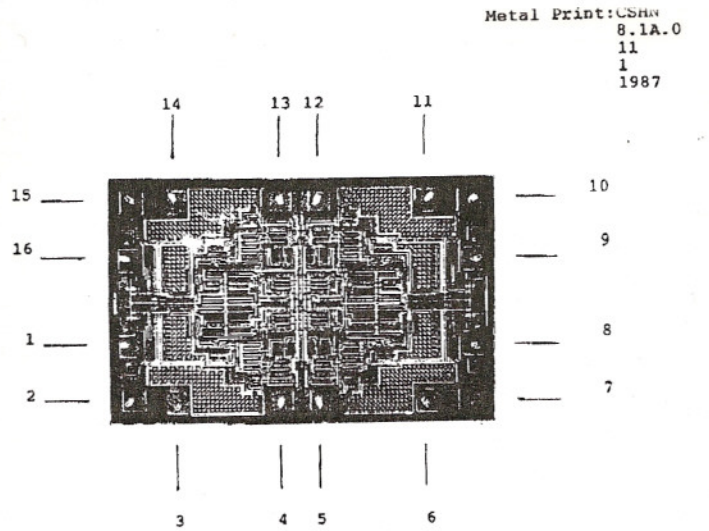
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PIN/PAD FUNCTION:

1. IN1	9. IN3	17.	25.
2. D1	10. D3	18.	26.
3. S1	11. S3	19.	27.
4. V-	12. VL	20.	28.
5. GND	13. V+(substrate)	21.	29.
6. S4	14. S2	22.	30.
7. D4	15. D2	23.	31.
8. IN4	16. IN2	24.	32.

Topside Metal: -
Backside: -
Backside Potential: V+
Mask Ref: -A
Bond Pads: .004”

APPROVED BY:CD	**DIE SIZE: .109” x .070”**	**DATE: 7/1/02**
MFG: Siliconix	**THICKNESS: -**	**P/N: DG411**